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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,568	09/24/2004	Chyh-Yih Chang	13216-US-PA	5567
31561	7590	02/27/2006	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2 TAIPEI, 100 TAIWAN			THOMAS, LUCY M	
			ART UNIT	PAPER NUMBER
			2836	

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/711,568	Applicant(s) CHANG, CHYH-YIH	
	Examiner Lucy Thomas	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 January 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13-20 is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings were received on 1/26/2006. These drawings are acceptable.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (US 6,618,230) in view of Gonthier (US 6,208,126). Regarding Claim 1, Liu et al. discloses a separated power electro-static discharge (ESD) protection circuit (Figures 1-6) coupled between a first power Line Vcc1 and a second power Line Vcc2, the separated power ESD protection circuit comprising: a first diode, having an anode and a cathode, wherein the anode is coupled to the first power Line (see Figure 3); a first metal-oxide-semiconductor (MOS) transistor, having a gate, a source and a drain (Figures 4), and a second diode, having an anode and a cathode, wherein the anode is coupled to the second power Line, the cathode is coupled to the first power Line (Figure 3). Liu et al. fails to disclose a first transistor first diode combination wherein, the drain is coupled to the cathode of the first diode and the source is coupled to the second power line. Gonthier discloses a first MOS transistor 30 and a first diode D1 combination (Figures 4 and 5) in a bidirectional switch device. It would have been

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obvious to those skilled in the art to modify Liu's circuit to replace a diode with a diode connected transistor as taught by Gonthier, because it is known in the art that the use of a diode connected transistor constitutes a parasitic silicon-controlled rectifier (SCR) and provides an effective static discharge route.

Regarding Claim 2, Liu et al. discloses a separated power ESD protection circuit, further comprising a second MOS transistor having a gate, a source and a drain, wherein the source is coupled to the first power line (Figure 4). Liu et al. fails to disclose a second transistor second diode combination wherein, the drain is coupled to the cathode of a second diode. Gonthier discloses a second MOS transistor 31 and a second diode D2 combination (Figures 4 and 5) in a bidirectional switch device. It would have been obvious to those skilled in the art to modify Liu's circuit to replace a diode with a diode connected transistor as taught by Gonthier, because it is known in the art that the use of a diode connected transistor constitutes a parasitic silicon-controlled rectifier (SCR) and provides an effective static discharge route. Claims 7 and 8 recites the elements of Claims 1 and 2 with additional elements of a plurality of first series diodes, and a plurality of second series diodes. Liu et al. discloses a plurality of first series diodes, and a plurality of second series diodes (Figure 3).

Regarding Claims 4, 6, 10, and 12, Liu et al. discloses a first MOS transistor, which is a P-type MOS transistor 28 as recited in Claim 4, and a second MOS transistor, which is a P-type MOS transistor 30 as recited in Claim 6 (Figure 6, Column 5, lines 1-16). Regarding Claims 3, 5, 9, and 11, Liu et al. fails to disclose a first MOS transistor, which is an N-type MOS transistor as recited in Claims 3 and 9, and a second

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MOS transistor, which is an N-type MOS transistor as recited in Claims 5 and 11. It would have been obvious to those skilled in art at the time the invention was made to provide a first N-type MOS transistor and a second N-type transistor and configure the circuit accordingly as N-type and P-type MOS transistors are art recognized equivalents.

Allowable Subject Matter

4. Claims 13-20 are allowed.
5. The following is a statement of reasons for the indication of allowable subject matter: Claims 13-20 recite an integrated circuit to protect internal circuits from electrostatic discharge using multiple ESD protection circuits, each comprising multiple diode strings and/or MOS transistor combination recited in Claim 13. The combined limitations are not disclosed by the Prior Art of Record, thereby rendering the claimed combination allowable.

Response to Arguments

6. Applicant's arguments filed 1/26/2006 have been fully considered.

The amendments to Claims 19-20 overcome the objections indicated under Claim Objections and Drawing Objections, set forth in this Office action dated 11/01/2005.

With regard to arguments directed toward the Gonthier reference, the Applicant states that Gonthier never disclosed any ESD protection circuit, and is neither in the field of applicant's field of endeavor nor reasonably pertinent to the particular problem with which was the inventor concerned. However, the Gonthier reference was relied upon solely to show the use of diode connected transistors. Gonthier teaches that diode connected transistors are known in the art, which is relevant knowledge to semiconductor circuit design in general, including but not limited to ESD protection circuits.

The Applicant states that it is not known in the art that the use of a diode connected transistor feature would form a parasitic silicon-controlled rectifier (SCR) for providing a static discharge route and that if it was known Liu would have disclosed this. However, it is not required that Liu or any base reference teach every claimed aspect of an invention. The Gonthier reference discloses the use of diode-connected transistors, which forms a parasitic SCR. Furthermore, Applicant's acknowledged Prior Art (Figure 4) also has a diode-connected transistor used as an ESD discharge route. The Liu reference also has noted the use of diode-connected devices for ESD discharge route (Column 1, lines 55-57). Therefore, it is believed that the rejection sufficiently meets the claimed limitations as the prior art provides the disclosure for using diode-connected transistors as ESD discharge paths.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lucy Thomas whose telephone number is 571-272-6002. The examiner can normally be reached on Monday - Friday 8:00 AM - 4:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LT

February 14, 2006



PHUONG T. VU
PRIMARY EXAMINER